Transistor Logic Example:

- Construct a NOR gate. Looks kind of familiar right?
- Remember: pMOS passes a strong 1, so should always be connected to $V_{dd}$
- How do we construct an OR? (add an inverter)
- On your own: design an AND gate
- Circuit symbols for what we’ve seen so far
- Symbols for what we’ve seen so far ($^* \, , \text{justaposition for AND; } \lor, + \text{ for OR}$)

Logical Expressions contd.

- Note AND is also called the “conjunction” of two expressions
- OR is called the “disjunction”
- Note that OR is inclusive. That is, $x \text{ OR } y$ is 1 when $x$ and $y$ are both 1
- We also have an exclusive version, appropriately named exclusive OR (XOR)
- Truth table:
  - $x \mid y \mid x \text{ XOR } y$
  - $\begin{array}{c|c|c}
  0 & 0 & 0 \\
  0 & 1 & 1 \\
  1 & 0 & 1 \\
  1 & 1 & 0
  \end{array}$
- Here, $x \text{ XOR } y$ is only one when $x \neq y$
- IMPLY $\implies$ conditional operator
  - $X \implies Y$ is 0 iff $X = 0$. Can be read “if $X$, then $Y$.” Note that $X \implies Y$ is the same thing as $\neg X \text{ OR } Y$ (by definition of implication)
- If we treat true and false numerically, then it also happens to be $X \leq Y$ (try it by making the truth tables)
- Equivalence (also called biconditional) - IFF (if and only if)
  - $X \iff Y = 1$ only when $X = Y$ ($X = 0 \text{ OR } Y = 0$ or $X = 1 \text{ AND } Y = 1$)
  - This also happens to be the opposite of XOR (so it is sometimes called XNOR). Hint: try pronouncing NXOR
- Operator symbols for XOR ($\oplus$), IMPL ($\implies, \rightarrow$), IFF ($\iff, \leftrightarrow$)
- Be careful with bars (not) $\overline{X \overline{Y}}$ is not same as $\overline{X} \overline{Y}$ (clear when drawn out)

Truth tables for larger expressions

- A truth table for an expression of $n$ variables has $n$ initial columns
- the remaining columns are for specific expressions
- For $n$ (binary) variables, how many rows will we have? ($2^n$)
- Once we have a truth table for an expression, it’s easy to determine logical equivalence of two expressions
• The truth tables are the same!
THE INVERTER

IN

V_{\text{DD}}

OUT

GATE SYMBOL

\overline{X} (or \overline{nx} or \overline{lX})
THE NAND GATE

RECALL

\[
\begin{array}{c|c|c}
X & Y & \text{NOT}XY \\
0 & 0 & 1 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]

PARALLEL

SERIES

GND

V_{DD}

OUT

(2)