

CS 471 - Design of Computer Processors

Last Updated – 05/01/2002

Course Manager - Virgil Bistriceanu, Instructor

3 credit hours; elective for CS, required for CPE; 100 min. lecture & 100 min. lab each week

Current Catalog Description - Further study of the internal design and organization of computer architectures. Methods of interconnecting devices: bus structures, independent channels, interrupt-driven controllers, synchronous and asynchronous devices. Survey of current microprocessors and microcomputer systems, including hardware/software interfacing and application of these systems. Hands-on experience in the construction of a microcomputer system. Prerequisite: CS 470. (2-2-3) (T) ???

Textbook

- James R. Armstrong, F. Gail Gray, *VHDL Design Representation and Synthesis*, Prentice Hall, 2000, ISBN 0-13-021670-4

References - other textbooks or materials

- Peter J. Ashenden, *The Designer's Guide to VHDL*, Morgan Kaufmann, ISBN 1-55860-270-4
- Jayaram Bhasker, *A VHDL Primer*, Prentice Hall, 1999, ISBN 0-13-096575-8
- David A. Patterson, John L. Hennessy, *Computer Organization and Design: the hardware/software interface*, 2nd edition, Morgan Kaufmann, Inc. 1994, ISBN 1-55860-491-X

Course Goals

- Become proficient in the use of the VHDL hardware description language
- Use Altera's VHDL software tools
- Design and simulate a significant digital design project

Students should be able to:

- Explain why formal models are needed:
 - Communicate requirements
 - Tool to document a system
 - Use simulation to allow for testing and verification of a design
 - Allow for formal verification of the correctness of a design
 - Allow automatic synthesis of circuits
- Domains and Levels of Modeling
 - Explain the difference between *function*, *structure* and *geometry* models of a system
- Explain what a Hardware Description Language (HDL) is and why it is needed
- Explain what VHDL stands for
- Explain the steps involved in writing the model of a system
 - Analysis
 - Elaboration
 - Execution
- Design, using VHDL, models for
 - Combinatorial circuits:
 - Binary adder
 - 1-bit ALU with arithmetic and logic operations
 - Comparator

- Barrel shifter
- Sequential circuits:
 - D-type register
 - Shift register
 - Asynchronous/synchronous counter
 - Finite Automata
- Create Test Benches:
 - Behavioral requirements
 - Timing requirements
 - Text I/O

Prerequisites by Topic

- Strong structured programming skills (C/Pascal) are required for this class as it involves the quick acquisition of a new programming language (VHDL). In addition, a good understanding of basic digital components (gates, Boolean functions, flip-flops, registers, counters, etc.) and their functionality is a must for successful completion of this class.

Major Topics Covered in Course

1. Fundamental Concepts	2 hours
2. Design & verification process	4 hours
3. VHDL Dataflow	4 hours
4. VHDL Behavioral	4 hours
5. VHDL Process	4 hours
6. VHDL Structural	2 hours
7. Test benches	4 hours
8. Development tools	2 hours
9. Synthesis & mapping algorithms	4 hours
10. Design for testability	4 hours
11. Case study	4 hours
Introduction: discuss class structure, objectives, and requirements, Midterm	3 hours
Final Exam	-
	? hours

Laboratory projects (specify number of weeks on each)

Exercises will include writing VHDL models of combinational and sequential circuits, synthesizing these models to FPGAs by automatic place and route, simulating the design, and developing and writing test-benches in VHDL

- Binary Adder, Logic Unit
- 7-Segment Display
- Digital Comparator

- Multiplier
- Sign extender
- 32-bit ALU (MIPS)
- Finite State Machine
- Barrel Shifter & Shifter
- Opcode decoder (MIPS)

Estimate CSAB Category Content in Credit Hours

	CORE	ADVANCED		CORE	ADVANCED
Data Structures			Computer Organization and Architecture		3
Algorithms			Concepts of Programming Languages		
Software Design					

Oral and Written Communications - Every student is required to submit at least __0__ written reports (not including exams, tests, quizzes, or commented programs) of typically __0__ pages and to make __0__ oral presentations of typically __0__ minutes duration. Include only material that is graded for grammar, spelling, style, and so forth, as well as for technical content, completeness, and accuracy.

- none

Social and Ethical Issues - Please list the topics that address the social and ethical implications of computing covered in all course sections. Estimate the class time spent on each topic. In what ways are the students in this course graded on their understanding of these topics (e.g., test questions, essays, oral presentations, and so forth)?

- none

Theoretical Foundations - Please list the types of theoretical material covered, and estimate the time devoted to such coverage in contact (lecture and lab) hours.

- VHDL Modeling, 8 hours

Problem Analysis - Please describe the problem analysis experiences common to all course sections.

- Test Benches, 4 hours

Solution Design - Please describe the design experiences common to all course sections.

Exercises will include writing VHDL models of combinational and sequential circuits, synthesizing these models to FPGAs by automatic place and route, simulating the design, and developing and writing test-benches in VHDL

- Binary Adder, Logic Unit
- 7-Segment Display
- Digital Comparator
- Multiplier
- Sign extender
- 32-bit ALU (MIPS)
- Finite State Machine
- Barrel Shifter & Shifter
- Opcode decoder (MIPS)

Other Course Information

- Planned Course Enhancements

- New Catalog Description: This course deals with the implementation aspects of Computer Architecture. An industrial standard hardware description language- VHDL (IEEE-1076) is introduced and the application of VHDL to top-down design methodology is presented. Hands-on experience in the design of key components of a CPU. Prerequisites: CS 350 or ECE 218. (2-2-3)